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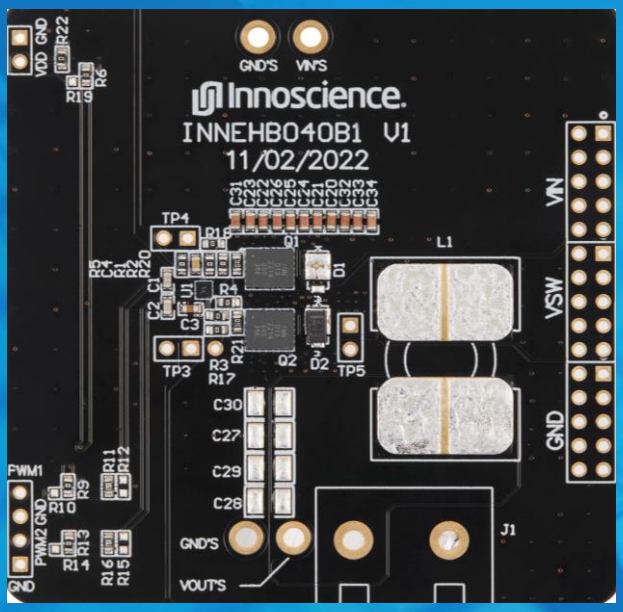
POWER THE FUTURE

INNEHB040B1

Evaluation Board Manual

40V GaN HEMT

Open Loop Half-Bridge EVB



CAUTION

Please carefully read the following content since it contains critical information about safety and the possible hazard it may cause by incorrect use.

ELECTRICAL SHOCK HAZARD

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

HOT SURFACE

The surface of PCB can be hot and could cause burns. DO NOT TOUCH THE PCB WHILE OPERATING!!

REMINDER

This product contains parts that are susceptible to electrostatic discharge (ESD).
When using this product, be sure to follow antistatic procedures.

List of Content

1. Overview

1.1. Introduction

INNEHB040B1 is a half-bridge evaluation board equipped with half-bridge gate driver to evaluate the performance of 40V GaN HEMT INN040LA015A. This board can simplify the test process, it can easily realize Buck or Boost converter with single or dual PWM input. The board includes all the necessary information you need, and the layout has been optimized to achieve the best performance. Test points are also included for the waveform measurement and efficiency evaluation.

1.2. Test Equipment Requirement

To evaluate the performance properly, you need to prepare the following test equipment:

1) High speed digital oscilloscope（>500MHz Bandwidth）
2) Low voltage DC power supply
3) PWM generator
4) Digital Multimeter
5) DC load (E-load or Power Resistor)

2. Performance Summary

Table 1 Electrical Characteristic（Ta=25℃）

Symbol	Parameters	Min	Nom	Max	Units
VDD	Gate Drive Regulator Supply Range	7		12	V
Vin	Input Voltage	0		32(1)	V
Fsw	Switching frequency		500		kHz
Pout	Output Power			180(2)	W
EFF	Typical efficiency		97.08%(3)		
Vpwm	Input Logic 'High'	3.5		5	V
	Input Logic 'Low'	0		1.5	V

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 40 V for INN040LA015A.

(2) Maximum output power depends on the thermal - actual maximum output power with be subject to switching frequency, bus voltage, load current and thermal cooling.

(3) 97.08% is the efficiency at 12V to 5V, load 15A, and frequency 500kHz.

3. Block Diagram

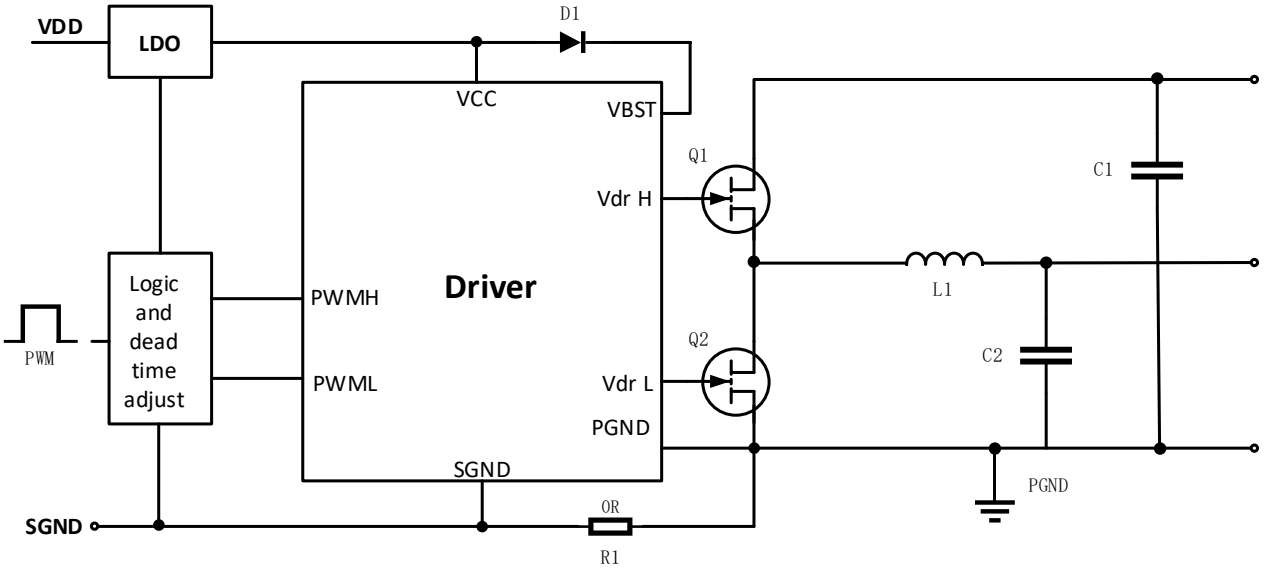


Figure 1 INNEHB040B1 Block Diagram

4. PCBA Overview and Schematic

4.1. PCBA Overview

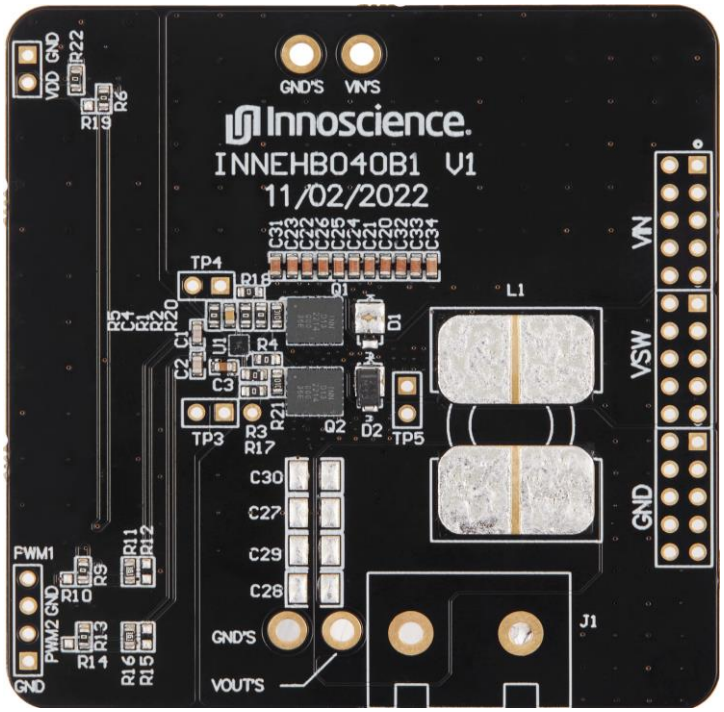


Figure 2 Top view of INNEHB040B1

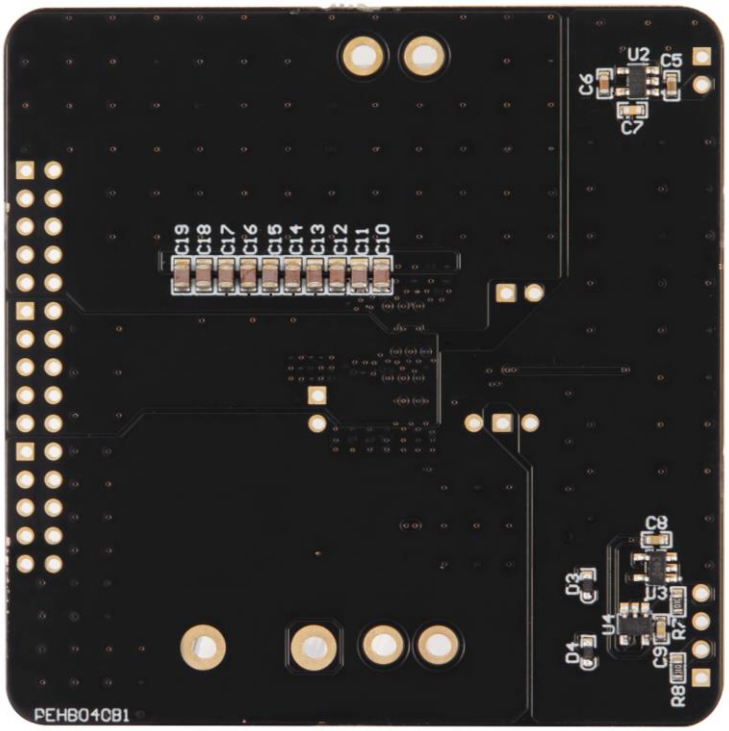


Figure 3 Bottom view of INNEHB040B1

4.2. Schematic

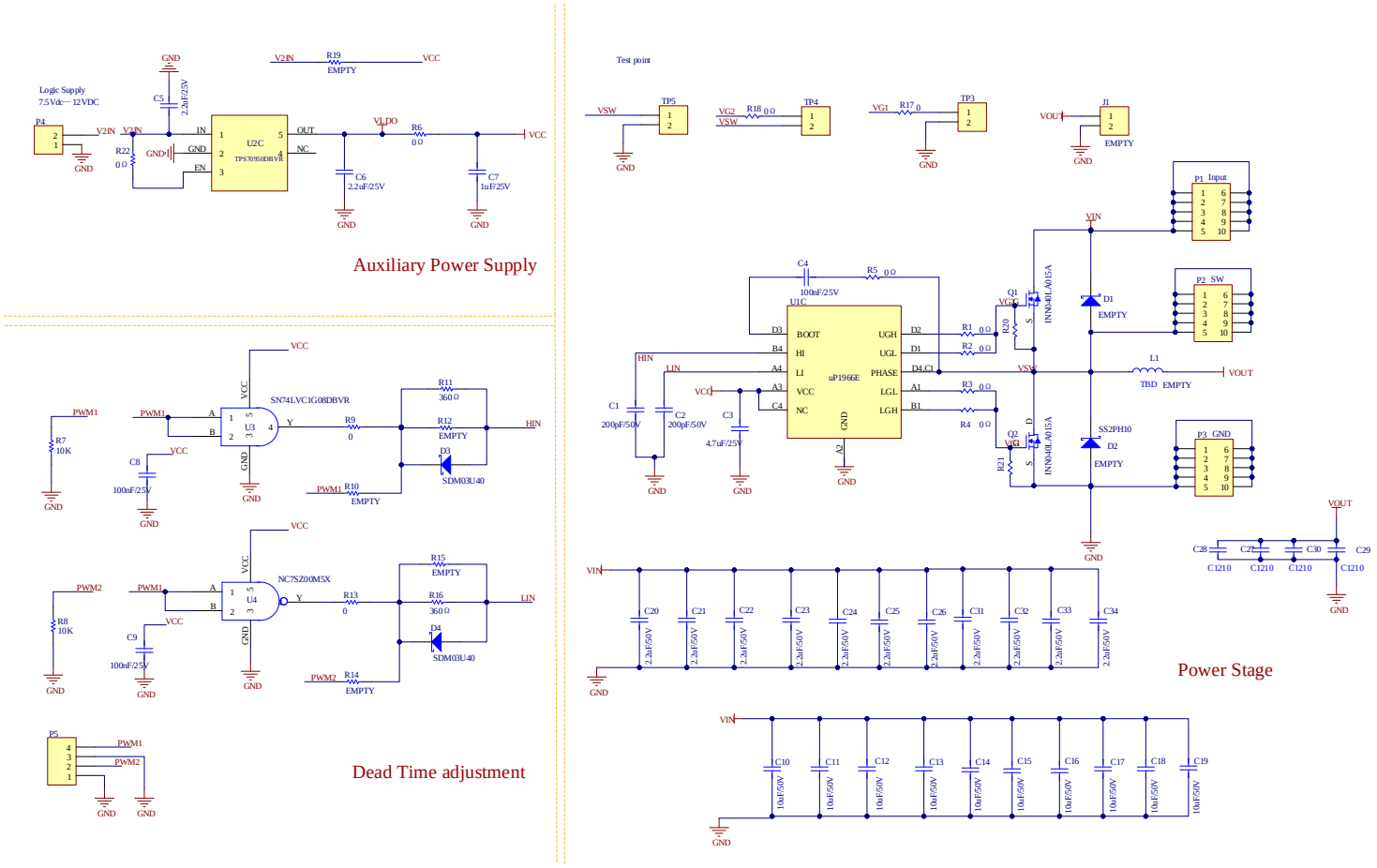


Figure 4 Schematic

5. Testing Guide

5.1. Test point location

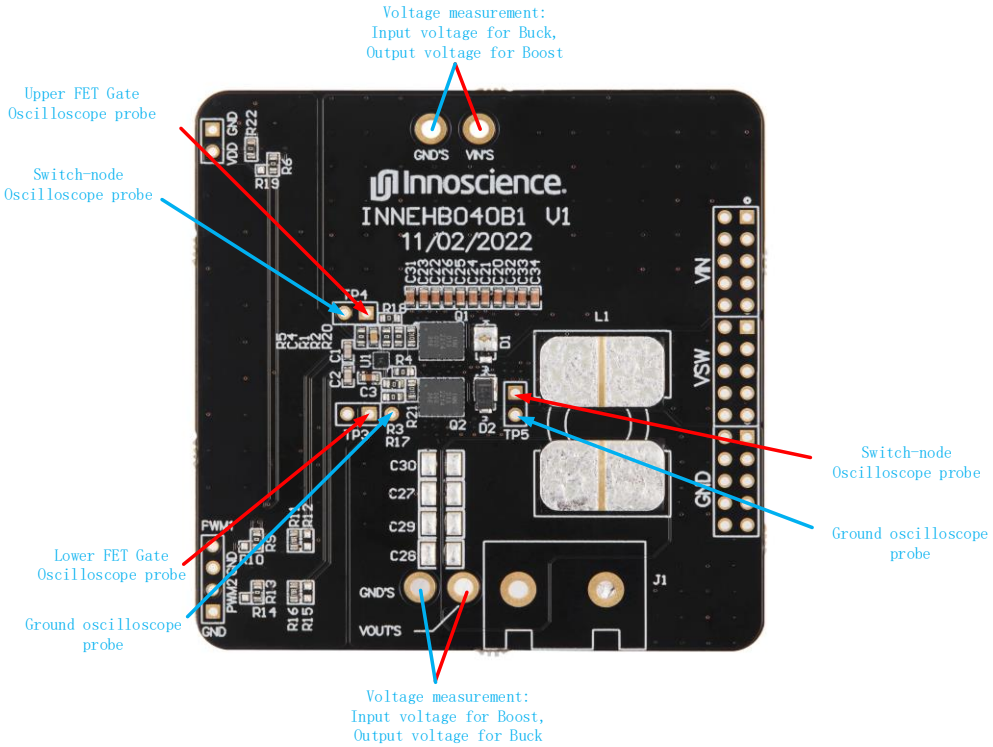


Figure 5 Measurement points

5.2. Test setup

5.2.1. Buck Mode

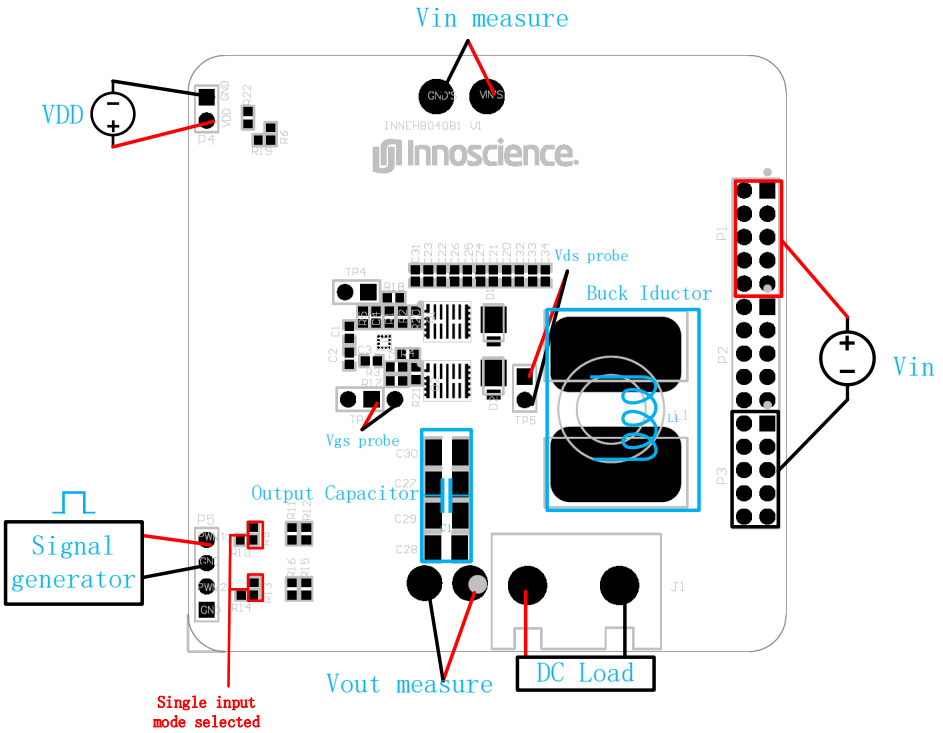


Figure 6 Single-PWM input Buck mode

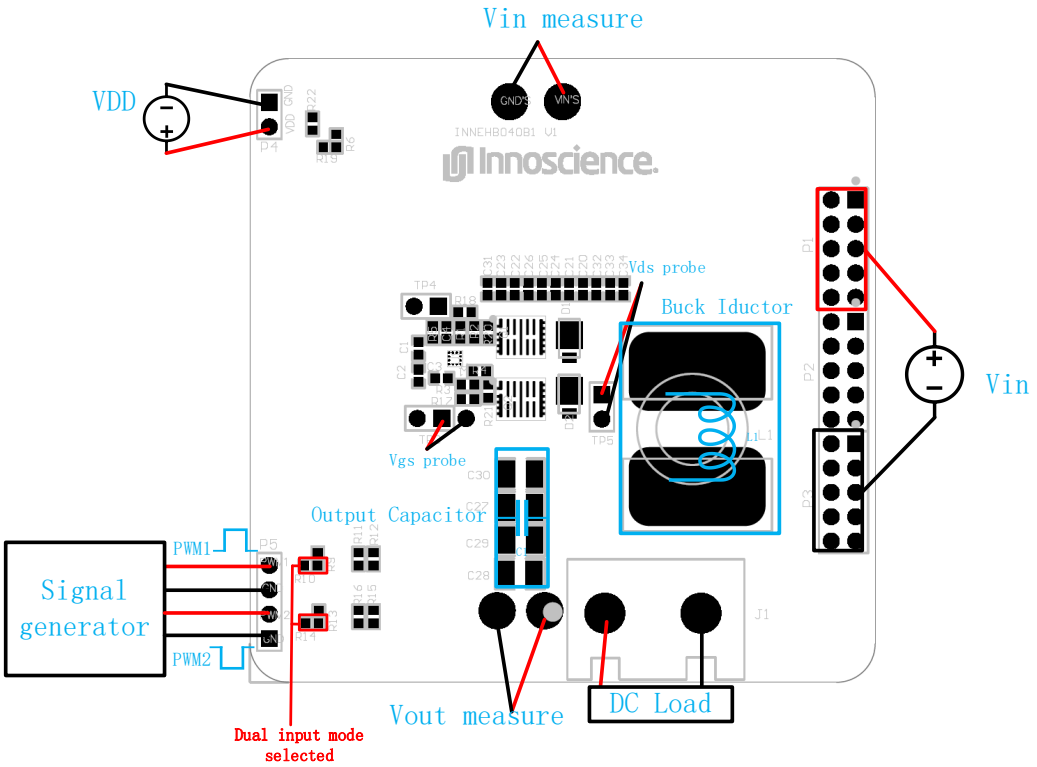


Figure 7 Dual-PWM input Buck mode

Before tests, single or dual PWM input modes could be selected. When selecting the single PWM input mode, please solder 0Ω resistor to R9 & R13. The dead time is regulated by R11, R16, C1 and C2. The default value for R11

and R16 is 360Ω, the value of C1 and C2 is 200 PF, and the corresponding dead interval is 25ns.

To select dual PWM mode, please solder 0Ω resistor to R10, R14, R11 and R16. Figure 7 Dual-PWM input Buck mode shows the required PWM signals; PWM1 and PWM2 should be complementary. The dead time is controlled by the signal generator.

5.2.2. Boost Mode

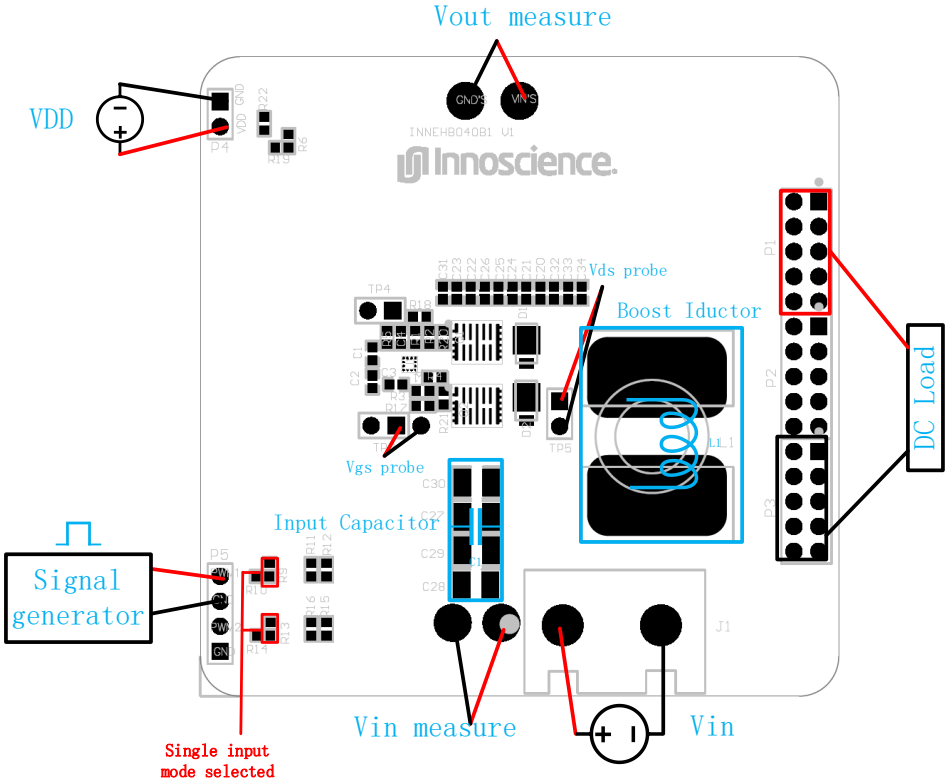


Figure 8 Single-PWM input Boost mode

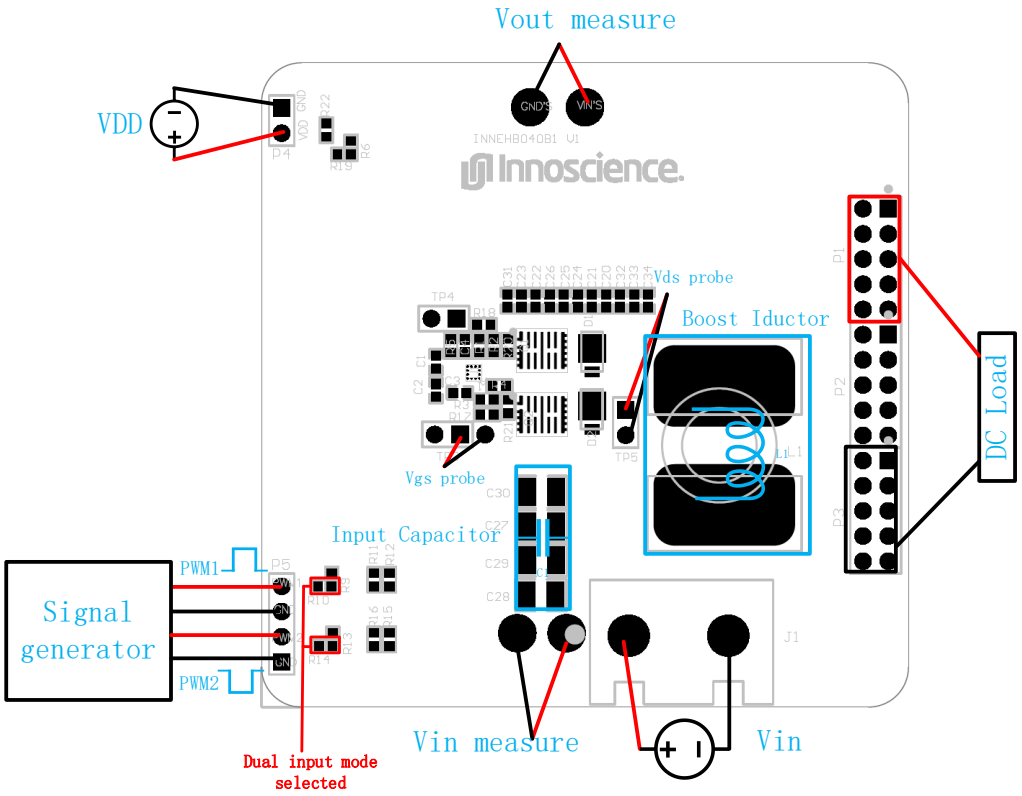


Figure9 Dual-PWM input Boost mode

5.3. Power up and down sequence

5.3.1. Power-up sequence (Buck Mode)

1. Check every power supply is **off.**
2. Connect the DC voltage source to VIN terminal **P1** and common ground GND terminal **P3**, as shown in Figure 6 (Pay attention to the polarity).
3. Connect the electronic load to pin **J1.**
4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).
5. Connect the signal generator to pin **P5**.
6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.
7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency .
8. Make sure the initial input supply voltage is 0 V, turn on the power and

slowly increase the voltage to the desired value (**do not exceed the absolute maximum voltage**). Probe switchnode and view the switching operation.

9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

5.3.2. Power-up sequence (Boost Mode)

1. Check every power supply is **off**
2. Connect the DC voltage source to pin **J1**, as shown in Figure 8 (Pay attention to the polarity).
3. Connect the positive pole of the electronic load to pin **P1** and the negative pole to pin **P3**.
4. Connect the auxiliary source to the VDD terminal **P4** (Pay attention to the polarity).
5. Connect the signal generator to pin **P5**.
6. Turn on the auxiliary power supply. Note the voltage ranges from 7V ~ 12V.
7. Open the signal generator and enter the PWM signal with the required duty ratio and frequency.
8. Make sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the desired value (**do not exceed the absolute maximum voltage**). Probe switchnode and view the switching operation.
9. Once operational, according to the heating state of the device slowly increase the load current, do not exceed the maximum temperature required by the device specification.

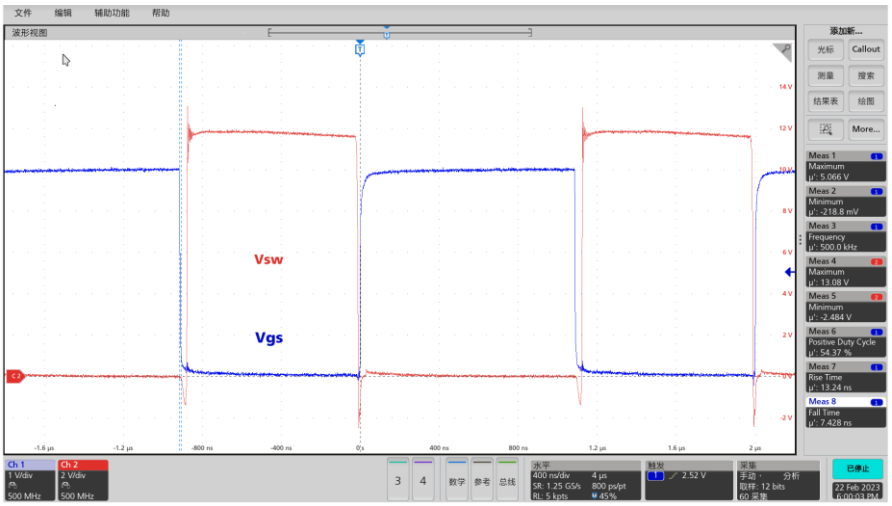
5.3.3. Power-down sequence

1. Turn off the **E-load** first
2. Turn off the **DC voltage source**

3. Turn off the **PWM generator**
4. Turn off the **auxiliary power supply**

6. Evaluation Results

6.1.1.Switching Waveforms (Rgon=0Ω, Rgoff=0Ω)



Test conditions

Vin=12Vdc

Vout=5Vdc

Iout=45A

fsw=500kHz

Airflow=1400LFM

Results

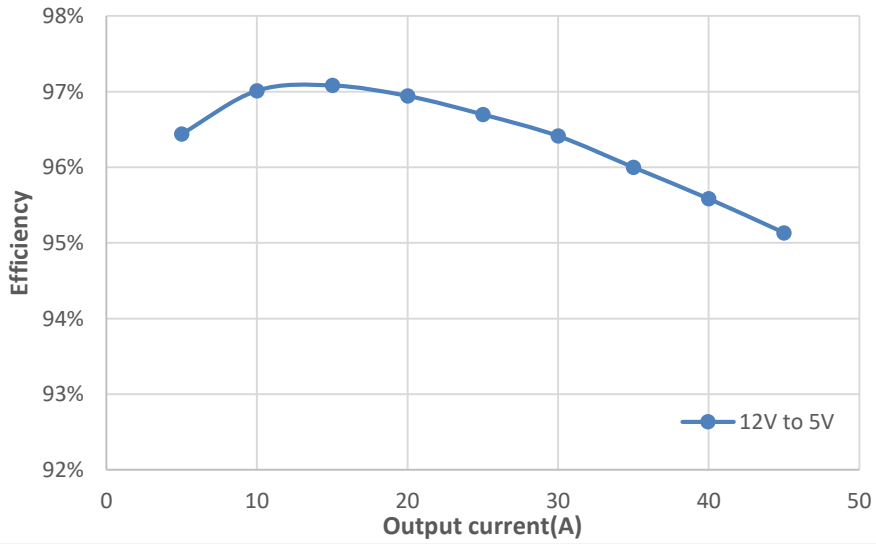
Vgsmax: 5.06V

Vsw overshoot: 1.08V

Vgs rising time: 13.24ns

Vgs falling time: 7.42ns

6.1.2.Efficiency Results

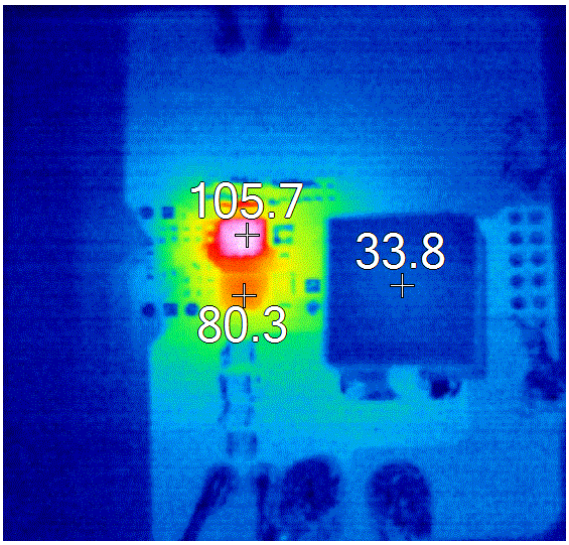


Test conditions

fsw=500kHz

Airflow=1400LFM

6.1.3.Thermal performance



Test conditions

Buck Mode

Vin=12Vdc

Vout=5Vdc

Iout=45A

fsw=500kHz

Airflow=1400LFM

Result

Switching GaN: 105.7℃

Continuation GaN: 80.3℃

Inductor: 33.8℃

Appendix

Appendix A. PCB Layout

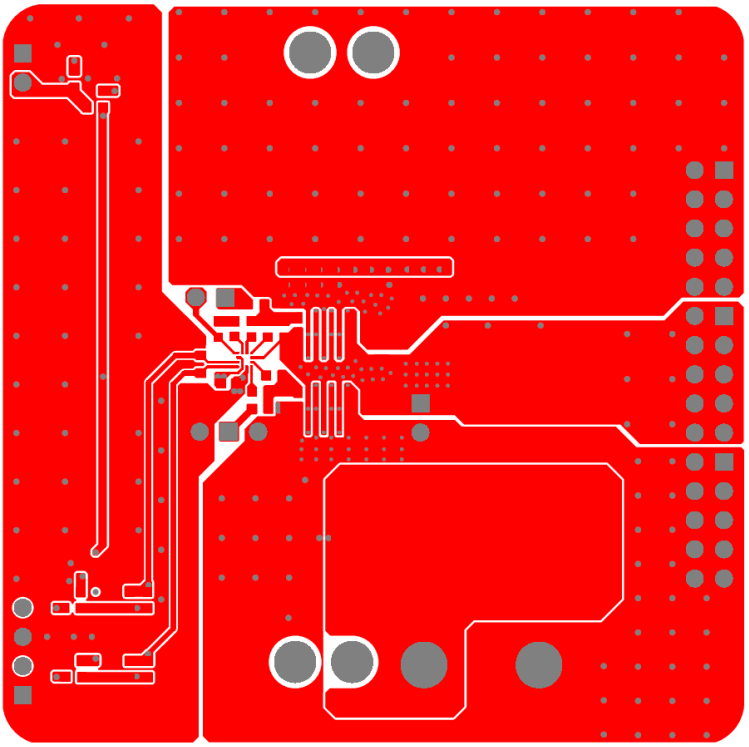


Figure 10 The top layer of INNEHB040B1

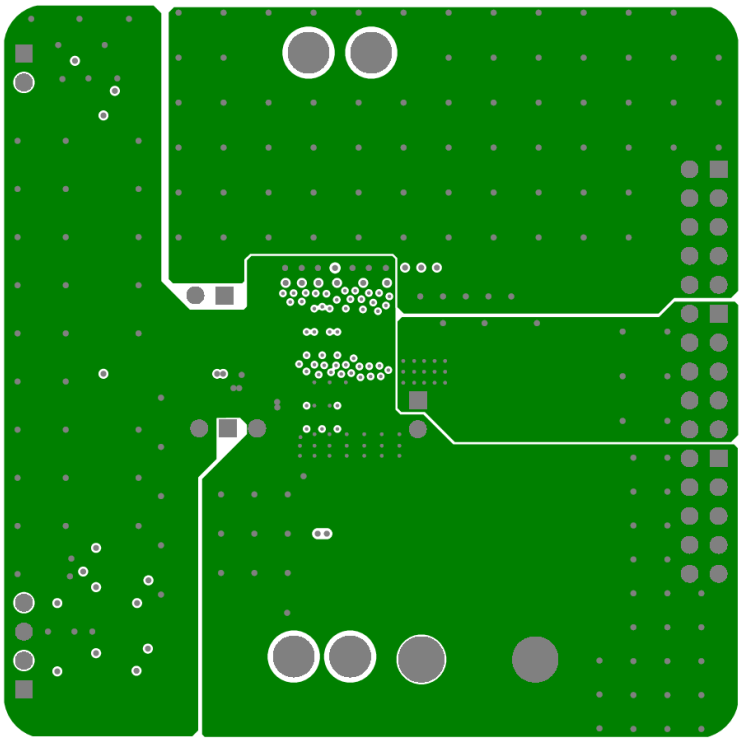


Figure 11 The first middle layer of INNEHB040B1

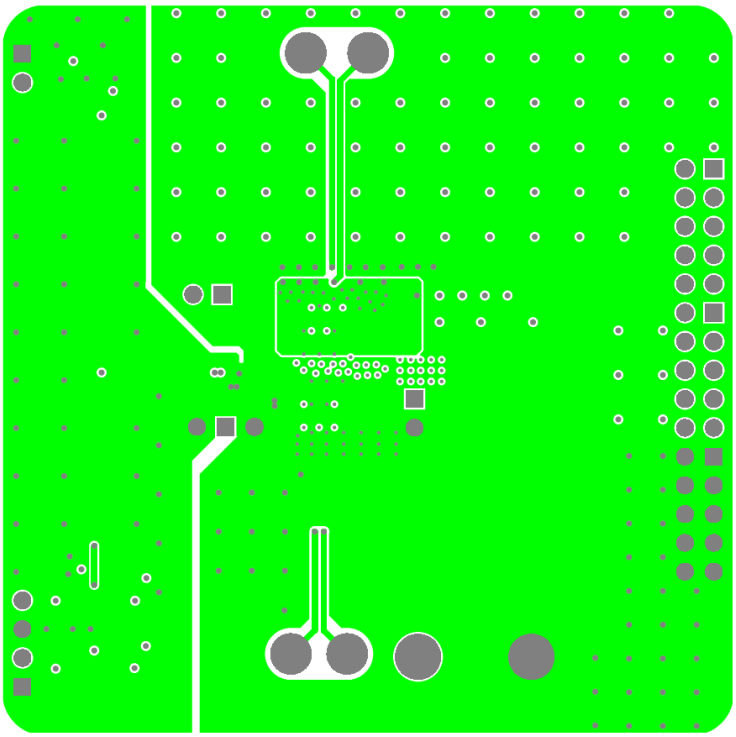


Figure 12 The second middle layer of INNEHB040B1

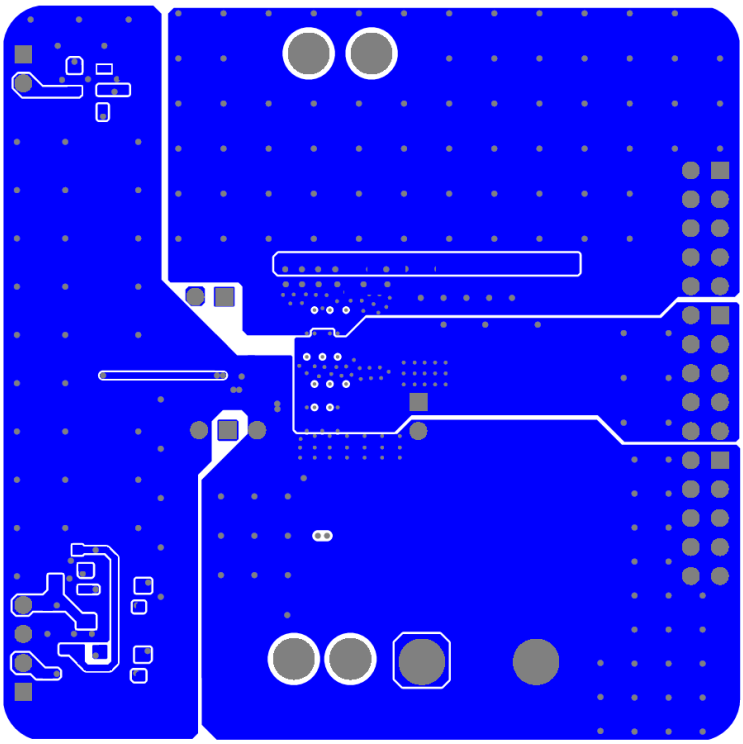


Figure 13 The bottom layer of INNEHB040B1

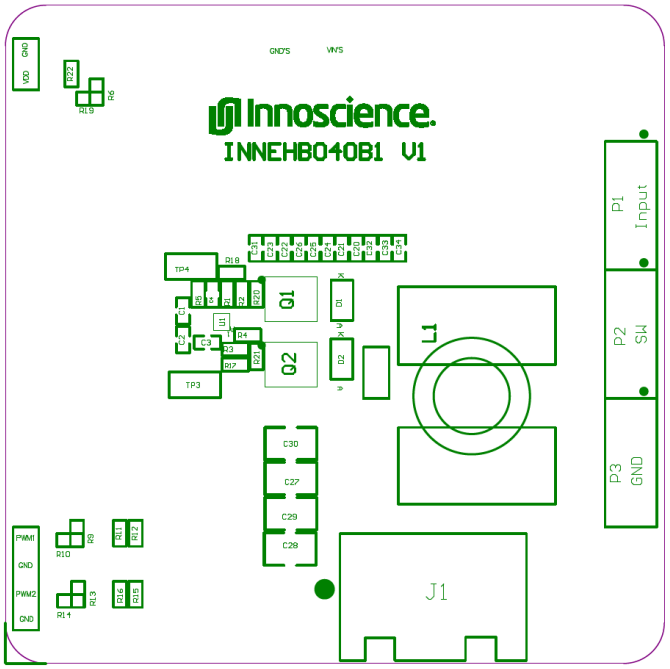


Figure 14 The top overlay of INNEHB040B1

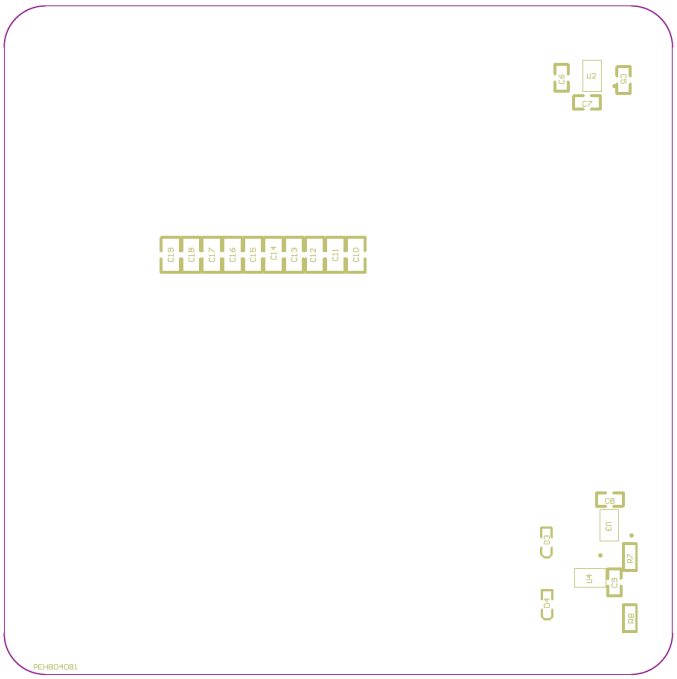


Figure 15 The bottom overlay of INNEHB040B1

Appendix B. BOM

Table 2 BOM

Designator	Part Number	Manufacturer	Description	Footprint	Quantity
C1, C2	0402N201J500CT	Walsin	CAP, 200pF/50V, ±5%, C0G	C0603	2
C3	TMK107BBJ475KA-T	TAIYO YUDEN	CAP, 4.7uF/25V, ±10%, X7R	C0603	1
C4，C8, C9	CC0603KRX7R8BB104	YAGEO	CAP, 100nF/25V, ±10%, X7R	C0603	3
C5, C6	CC0603KRX5R8BB225	YAGEO	CAP, 2.2uF/25V, ±10%, X5R	C0603	2
C7	TMK107BJ105KA-T	TAIYO YUDEN	CAP, 1uF/25V, ±10%, X7R	C0603	1
C10, C11, C12, C13, C14, C15, C16, C17, C18, C19	GRM21BR61H106KE43L	muRata	CAP,10uF/50V, ±10%, X5R	C0805	10
C20, C21, C22, C23, C24, C25, C26，C31，C32，C33，C34	GRM188R61H225KE11D	muRata	CAP,2.2uF/50V, ±10%, X5R	C0603	11
C27, C28, C29, C30	EMPTY		cap	C1210	4
D1	EMPTY				1
D2	SS2PH10	VISHAY	Schottky Diode，100V，2A，	SMP(DO-220AA)	1
D3, D4	SDM03U40	DIODES	Schottky Diode，30V，0.3A，	SOD-523	2
L1	EMPTY		Inductance		1
Q1, Q2	INN040LA015A	Innoscience	GAN FETs，40V/1.5mΩ，	FCLGA 5mm×4mm	2
R1,R2, R3，R4，R5,R6,R9, R13，R17,R18，R22	ERJ3GEY0R00V	PANASONIC	Chip resistors，0Ω，100mW，0603	R0603	11
R7, R8，R20, R21	ERA2AED103X	PANASONIC	Chip resistors，10KΩ，±0.1%，0603	R0603	4
R10, R12, R14, R15, R19	EMPTY		Chip resistors，EMPTY，	R0603	5
R11，R16	0603WAF3600T5E	UNI-ROYAL	Chip resistors，360Ω，±1%，0603	R0603	2
U1	uP1966E	uPI Semiconductor	Dual-Channel Gate Driver	WLCSP1.6x1.6-12B	1

U2	TPS70950DBVR-TP	TECH PUBLIC	LDO voltage regulators , fixed 5V output,	SOT-23	1
U3	SN74LVC1G08DBVR	Texas Instruments	Single 2-Input Positive-AND Gate	SOT-23	1
U4	NC7SZ00M5X	Onsemi	Two-Input NAND Gate	SC-74A	1

Revision History

Date	Author	Versions	Description	Check
2/23/2023	MiaoSong	1.0	First edition	AE Team
8/8/2023	MiaoSong	1.1	Update Schematic and PCB Overlay	AE Team

Note:
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